HYBRID PULSE-AMPLITUDE-MODULATION SIGNALING SCHEME AND CLOCK SYNTHESIS FOR NEXT GENERATION ULTRA-HIGH-SPEED WIRE-LINE RECEIVERS

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HYBRID PULSE-AMPLITUDE-MODULATION SIGNALING SCHEME AND CLOCK SYNTHESIS FOR NEXT GENERATION ULTRA-HIGH-SPEED WIRE-LINE RECEIVERS

by

Asif Wahid

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STATEMENT OF DISSERTATION APPROVAL

The dissertation of **Asif Wahid**

has been approved by the following supervisory committee members:

Seyed Armin Tajalli	, Chair	**03/26/2024**
		Date Approved
Behrouz Farhang	, Member	**03/26/2024**
		Date Approved
Cynthia Furse	, Member	**03/26/2024**
		Date Approved
Ross Walker	, Member	**03/26/2024**
		Date Approved
Gain Kim	, Member	**03/26/2024**
		Date Approved

and by **Hanseup Kim**, Chair of

the Department of **Electrical and Computer Engineering**

and by **Darryl P. Butt**, Dean of The Graduate School.

ABSTRACT

High-speed and low-energy data movement are vital in modern High-Performance Computing (HPC) systems. The bandwidth (BW) for transferring data among different processing components in an HPC system directly affects the overall performance of such systems. The requirement for high-speed data transfer has further increased due to the advent of data-driven fields where low latency is an absolute necessity, such as Machine Learning, Artificial Intelligence, and Autonomous Driving. Advanced serial data communication systems and architectures have been proposed to address the growing demand for data transfer BW at lower energy consumption. The thesis introduces a signaling strategy aimed at addressing the inherent trade-off between achieving high data throughput and implementing an energy-efficient receiver system. Furthermore, it investigates the necessity of a low-jitter, high-bandwidth Phase-Locked Loop (PLL) for serial link systems. Two PLL prototypes with distinct architectures are presented to achieve sub-100fs root mean square (rms) jitter performance, a crucial requirement for precise clocking in wireline communication systems. In addition to providing a theoretical explanation of the bandwidth extension technique, the thesis presents measurement results of the fabricated PLL chips, demonstrating close alignment with simulation results and validating the claimed bandwidth extension technique. The report also delves into a systematic design approach for analyzing the noise performance of an oscillator, a fundamental component of the PLL and essential for clean clock design. Finally, the report showcases the application of the PLL in solving power flow issues in a grid network through the development of an analog emulator. The main goal of this work is to develop proper signaling schemes, circuit topologies, and architecture with a focus on the receiver side targeting high throughput chip-to-chip communication.

I dedicate this thesis to the woman whose unwavering love and encouragement have been my guiding lights—my mother.

CONTENTS

LIST OF TABLES

NOTATION AND SYMBOLS

IoT	Internet of Things
SoC	System On Chip
CPU	Central Processing Unit
NoC	Network On Chip
PCIe	Peripheral Component Interconnect Express
PAM	Pulse Amplitude Modulation
HMT	Hadamart Multi-Tone
PLL	Phase-Locked-Loop
ISI	Inter-Symbol-Interference
UI	Unit-Interval
SNR	Signal-to-Noise Ratio
MIC	Multi-Input Comparator
NRZ	Non-Return-to-Zero
ENRZ	Ensemble Non-Return-to-Zero
CNRZ	Correlated Non-Return-to-Zero
XTALK	Cross-Talk
CMN	Common-Mode Noise
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
DIMM	Dual In-Line Memory Module
PCB	Printed Circuit Board
MDB	Multi-Drop Bus
DMT	Discrete-Multi-Tone
OFDM	Orthogonal Frequency Domain Multiplexing
DSP	Digital-Signal-Processing
FEC	Forward-Error Correction
FIR	Finite Impulse Response
FFE	Feed-Forward Equalizer
DFE	Decision Feedback Equalizer
MCM	Multi-Chip-Module
BER	Bit-Error-Rate
EH	Eye Height
EW	Eye Width
RJ	Random Jitter
DJ	Deterministic Jitter
ENOB	Effective Number of Bit
CTLE	Continuous Time Linear Equalizer
UCIe	Universal Chiplet Interconnect Express
AMT	Analog Multi-Tone
BB	Base-Band

PRBS	Pseudo-Random Binary Sequence
BW	Bandwidth
TX	Transmitter
RX	Receiver
FOM	Figure of Merit
PFDxCPC	Phase Frequency Detector and Charge Pump Circuit
VCO	Voltage-Controlled-Oscillator
ECL	Emitter-Coupled-Logic
DCD	Duty-Cycle-Distortion
CP	Charge Pump
SP	Single Phase
DP	Double Phase
CML	Current Mode Logic
SOI	Silicon-On-Insulator
SSPLL	Sub-Sampling Phase Locked Loop
FLA	Frequency Lock Acquisition
DTPD	Discrete-Time Phase Detector
PN	Phase Noise
GBW	Gain Bandwidth
RO	Ring Oscillator
AMU	Analog Emulator Unit
AEM	Analog Emulator
PI	Phase Interpolator
XTAl	Crystal Oscillator
DCA	Digitally Controlled Amplifier
PD	Peak Detector
SAR	Successive Approximate Register
FSM	Finite State Machine
CDR	Clock Data Recovery

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