HYBRID PULSE-AMPLITUDE-MODULATION SIGNALING SCHEME AND CLOCK SYNTHESIS FOR NEXT GENERATION ULTRA-HIGH-SPEED WIRE-LINE TRANSMITTERS

by

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STATEMENT OF DISSERTATION APPROVAL

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ABSTRACT

High-speed and low-energy data movement is vital in modern High-Performance Computing (HPC) systems. The bandwidth (BW) for transferring data among different processing components in an HPC system directly affects the overall performance of such systems. The requirement for high-speed data transfer has further increased due to the advent of data-driven fields where low latency is an absolute necessity, such as Machine Learning, Artificial Intelligence, and Autonomous Driving. Advanced serial data communication systems and architectures have been proposed to address the growing demand for data transfer BW at lower energy consumption. More complex equalization schemes, such as high-order decision-feedback and feed-forward equalizers (DFE and FFEs), combined with analog-to-digital (ADC) based receivers are proposed to maximize the benefit from technology scaling and enhance the throughput of the chip-to-chip links. The main goal of this work is to develop proper signaling schemes, circuit topology, and architecture with a focus on the transmitter side targeting high throughput chip-to-chip communication.

A hybrid PAM and time domain multi-tone signaling scheme has been proposed and investigated with targeting high throughput and efficiency. The scheme combines multiple aspects of a signal including Pulse Amplitude Modulation (PAM), orthogonal multi-tone, and spatial modulation to achieve this. Focusing on the transmitter, the signaling has been realized, designed at the transistor level, and compared to contemporary schemes showing up to 3x improvement in efficiency, consuming 273 fJ/b transmitting at 120 Gb/s/pair of channels. Towards implementing it in a full SerDes system, low noise high-frequency clock generation has been identified as the key blocker. Therefore, significant design and fabrication efforts have been diverted to the design of an ultra-low phase noise Phase Locked Loop (PLL). Through 2 generations of development, a 26 fs-rms PLL has been fabricated and tested.

CONTENTS

APPENDICES

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APPENDIX B

THESIS JOURNEY: RESEARCH, INTELLECTUAL PROPERTY AND DISSEMINATION ENDEAVORS

B.1 Publications

- R. Bindiganavile and A. Tajalli, "Spectrum-Efficient Communication Over Copper Using Hybrid Amplitude and Spatial Signaling," in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Dallas, TX, USA, 2019, pp. 1061-1064, doi: 10.1109/MWSCAS.2019.8884807.

- A. Wahid, R. Bindiganavile and A. Tajalli, "Optimal PAM Order for Wireline Communication," in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401371.

- R. Bindiganavile and A. Tajalli, "A Controllable KVCO Ring VCO Topology," in *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Lansing, MI, USA, 2021, pp. 732-736, doi: 10.1109/MWSCAS47672.2021.9531824.

- R. Bindiganavile, A. Wahid, J. Atkinson and A. Tajalli, "A 59 fsrms 35 GHz PLL with FoM of -241 dB in 0.18μm BiCMOS/SiGe Technology," in *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, CO, USA, 2022, pp. 163-166, doi: 10.1109/RFIC54546.2022.9863116.

- A. Wahid, J. Atkinson, R. Bindiganavile, F. Jazaeri and A. Tajalli, "Noise-Aware FET Circuit Design Based on C/ID-Invariant," in *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, vol. 70, no. 7, pp. 2330-2334, July 2023, doi: 10.1109/TCSII.2023.3242209.

- R. Bindiganavile, A. Wahid and A. Tajalli, "A 29 GHz Sub-Sampling PLL with 25.6-fs-rms RJ based on a Discrete-Time Integrating PD in 45nm RF SOI," in *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, CO, USA, 2024, Accepted.

- A. Wahid, R. Bindiganavile and A. Tajalli, "Hadamard Multi-Tone Signaling in Multi-Wire Pulse Amplitude Modulation for Next Generation Wireline Communication," in *2024 IEEE International Symposium on Circuits & Systems (ISCAS)*, Singapore, 2024, Accepted.

- R. Bindiganavile, A. Wahid and A. Tajalli, "Trade-Offs in Design of Low-Jitter and Wideband Phase-Locked Loops," in *IEEE Journal of Solid-State Circuits (JSSC)*, Accepted Submission & Under-Review.

- R. Bindiganavile, A. Wahid and A. Tajalli, "A 29 GHz Sub-Sampling PLL with 25.6-fs-rms RJ based on a Discrete-Time Integrating PD in 45nm RF SOI," in *IEEE Journal of Solid-State Circuits (JSSC)*, Planned Extension/Under-Consideration.

B.2 Presented Posters and Letters

- R. Bindiganavile and A. Tajalli, "Towards Tb/s/mm communication Over Copper," in *Silicon Photonics for High-Performance Computing (SPHPC)*, 2019, Estes Park, CO, USA.

- R. Bindiganavile, A. Wahid, J. Atkinson, and A. Tajalli, "A Wideband Matrix Phase Detection PLL with Very Low Phase Noise in SiGe," in *Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, 2021.

- R. Bindiganavile, A. Wahid, J. Atkinson, S. Swearngin, and A. Tajalli, "Wideband PLL for Low Phase-Noise Frequency Synthesis," in *Electronics Resurgence Initiative (ERI) Summit*, 2021.

- J. Atkinson, A. Adair, S. Kalidasan, B. Jamadi, A. Wahid, R. Bindiganavile, and A. Tajalli, "CID: A Generalized Analog Design Methodology," in *Western Regional Electrical and Computer Engineering Department Head Association (ECEDHA)*, Salt Lake City, October 2022.

B.3 Designed ICs, Fabricated and Supported Tape-outs

- A 29 GHz Sub-Sampling PLL with 26 fs-rms jitter in 45 nm SiGe BiCMOS (Model, Design, Layout).
- A 35 GHz PLL with 59 fs-rms jitter in 0.18μm SiGe BiCMOS (Model, Design, Layout).
- An extreme-low power 200 fW/stage 1 kHz CMOS ring oscillator in 28nm CMOS (Design, Layout).
- A high-throughput SerDes transmitter in CMOS 28 nm using a Hybrid Multi-Tone / PAM signaling (Transmitter; Model, Design).
- Developed a signaling scheme and bandwidth-extending matching network for a short-reach SerDes link (Design).
- Provided technical support in layout design for the fabrication process and C/ID methodology evaluation blocks in 0.18μm SiGe BiCMOS and 45 nm SiGe BiCMOS.
- Provided technical support in the layout design of an Analog Neural Network accelerator test chip in 28 nm CMOS.

B.4 Patent

- R. Bindiganavile, A. Wahid, J. Atkinson, and A. Tajalli, "A Wide-Band Multi-Phase Phase-Locked Loop Circuit," App. No. PCT/US2023/068559.

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