Algorithmic Analog Design
C/ID: A Design Oriented FET Modeling and Design Approach

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Outline

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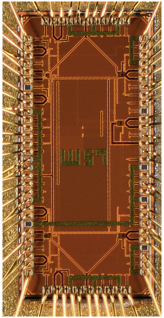
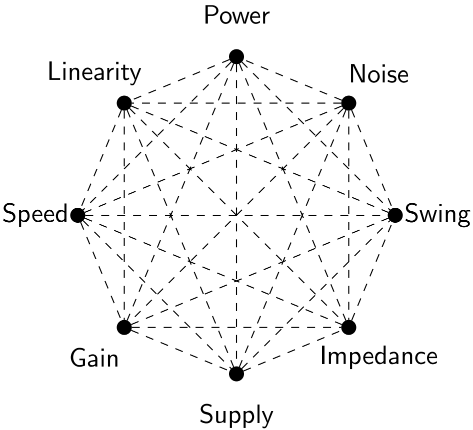
Application Area

- Analog integrated circuits are key elements in the modern industry:
  - Communications (e.g., wireless),
  - Computing (e.g., wireline links, clock generators, power management)
  - Sensor interfaces and healthcare (e.g., data converters)
  - Consumer (e.g., data converters, power management, protection)
  - Emerging applications (e.g., machine learning, quantum computing)



Design Space

- Complex design space makes it challenging to devise concise and efficient design algorithms.



Razavi's octagonal design space illustration [1].

Challenges and Complexities

Problem Description

Process of design, layout, and verification of analog circuits are complex, time consuming, prone to error, and very costly for industry.

State-of-the-Art: Tools

Tool/Framework	Description
ALIGN	Analog Layout, Intelligently Generated from Netlists. Developed under the DARPA IDEA program by the University of Minnesota, Texas A&M University, and Intel Corporation[2]
BAG	Berkeley Analog Generator
AutoCkt	A reinforcement learning-based framework
MAGICAL	An automatic layout generation tool
AIDA	Analog IC Design Automation, a commercial framework that assists expert analog IC designers
Synopsys ASO.ai	Design accelerator (implementation, and verification)
MunEDA WiCkeD	Circuit optimization and sizing tool suite, using machine learning [3]

State-of-the-Art: Algorithms

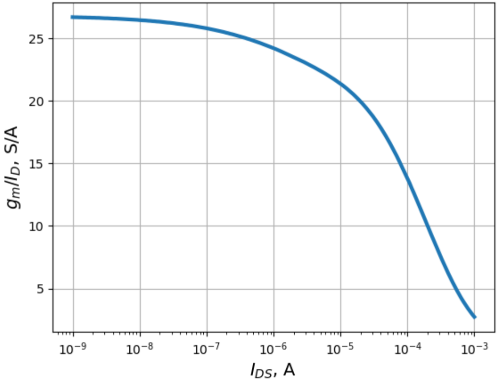
Method	**Description**	Ref.
g_m/I_D	Develop in 90s at KUL (Belgium) and Stanford (USA)	[4], [5]
IC	Inversion Coefficient, developed in 90s at EPFL (Switzerland)	[6]
C/I_D	Developed around 2018 at the University of Utah (USA)	[7]–[14]

Remark

More than 50 years after invention of FET devices, still there are fundamental problems related to basic circuit design with no straightforward solution.

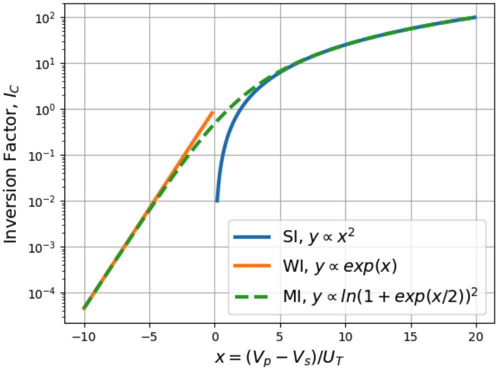
State-of-the-Art: Algorithms - gm/ID

- In 1996, Silveira et al. claimed that $\mathcal{G}_m = g_m/I_D$ can be used as a design variable [5].
- Next step, look-up table based design approaches were proposed.



State-of-the-Art: Algorithms - EKV

- In 1995, EKV proposed a mathematical interpolation to adequately model weak-, medium-, and strong-inversion regions [6].
- Smooth transition between different modes of operation of FET devices, make it convenient for device modeling and simulation.

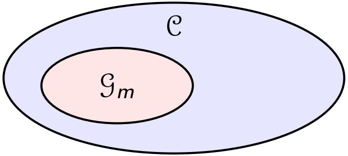


Aims

Aim of This Work

Develop a human comprehensive design algorithm:

- Analytical, but yet based on simple Mathematical rigour.
- Including complexities of FET devices, but in a concise way, that does not distract designers from the main flow.



Generalized design methodology, from $\mathcal{G}_m$ design space to $\mathcal{C}$.

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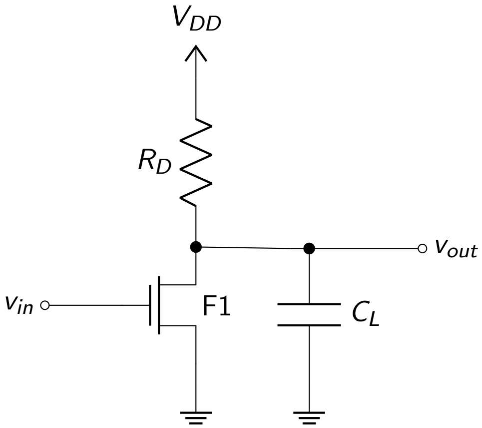
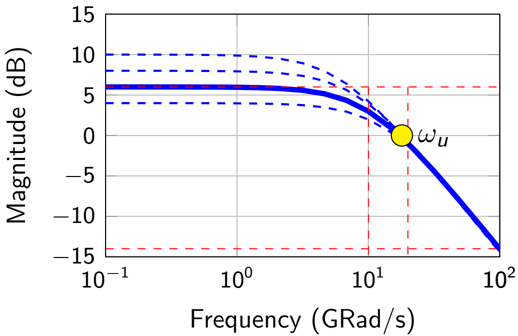
Fundamental Question

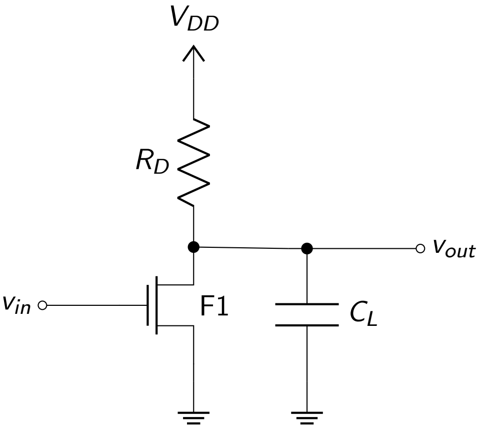
- Let's look into one of the most fundamental design questions in the field of analog circuits.
- Problem Description: What is the minimum level of energy consumed by a FET[a] circuit, to perform the most basic linear algebraic operation, i.e., $y = a \cdot x$.
- Dot product is a very fundamental operator, such as in neural networks and machine learning, among others.



[a] Field Effect Transistor

Fundamental Question





Unity gain-bandwidth product, $\omega_u = 2\pi GWB$, indicates how fast your circuit can operate before failing.

Fundamental Question: Approaching Problem

- Energy (or power) dissipation of an electronic circuit is a direct function of its performance, especially its operating speed.

$$\omega_u = \frac{g_m}{C}$$

- ω_u: Unity gain-bandwidth product,
- g_m: Transistor's characteristics parameter, i.e., transconductance,
- C: Circuit's bandwidth limiting factor, i.e., load capacitance.

Fundamental Question: Issues

$$\omega_u = \frac{g_m}{C}$$

- The good news is that the underlying equation governing power vs operating speed of an analog circuit is very simple.
- The first issue here is that this equation does not directly provide hints regarding power dissipation of the circuit.
- The second issue is that this equation does not have a closed form solution, due to complexities of device physics.
  - g_m and self-loading capacitance of transistor, C_S, are functions of device operating points and its dimensions, not presentable in a closed-form.

Fundamental Question: Step-by-Step Approach

- Before focusing on complexities of device physics, let's focus on how to bring in power dissipation into picture.

$$\omega_u = \frac{\mathcal{G}_m \times I_{DS}}{C}$$

- A simple mathematical parameter exchange, i.e., replacing g_m with transconductance-efficiency, $\mathcal{G}_m = g_m/I_{DS}$, does the job.

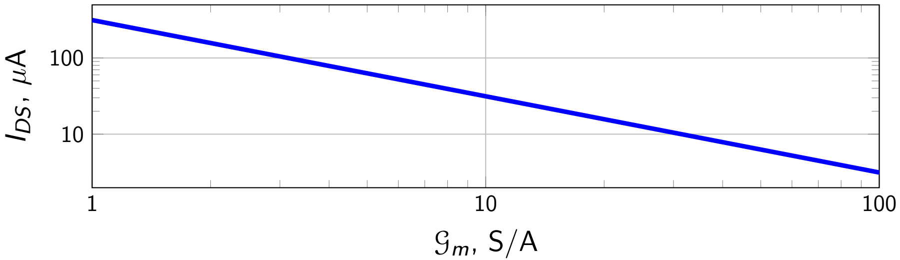
Fundamental Question: Step-by-Step Approach

- Consider now $\mathcal{G}_m$ as a fundamental design parameter:

$$I_{DS} = \frac{\omega_u \times C}{\mathcal{G}_m} \propto P_{diss}$$

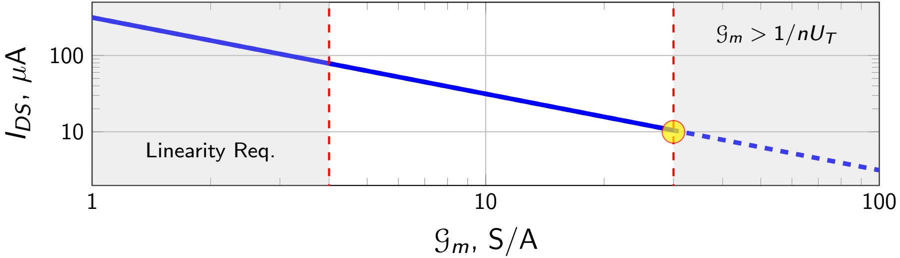
Low $\mathcal{G}_m$	Medium $\mathcal{G}_m$	High $\mathcal{G}_m$
High-Speed	Balanced Design	Low-Power

Fundamental Question: Design Space



- Observation: The underlying relationship between power and operating speed is rather simple if self-loading capacitance of the FET device is ignored.
- Guideline: Increasing $\mathcal{G}_m$ helps to reduce circuit power consumption, *though this sentence is not always correct*.

Fundamental Question: Design Space



- Note: Transconductance-efficiency has a physical upper limit, that depends on device sub-threshold slope factor, n and thermal voltage, $\mathrm{U_T}$.
- Note: The lower limit on transconductance-efficiency depends on supply voltage, circuit linearity requirements, device breakdown voltage, or electro-migration (current density).

Summary

- Speed vs power dissipation trade-off can be the opening door toward solving a classic problem, i.e., energy consumption in computing systems.
- FET device model complexities limits our observability on design space. As a result, packing all the model-related complexities under a very limited number of device parameters is highly desirable.
- To reveal the relationship between power and speed, using $\mathrm{g_m/I_{DS}}$ is essential.
- Vision: Use $\mathrm{I_{DS}}$ vs $\mathrm{g_m/I_{DS}}$ as the fundamental design space, and map different design specs to that space.

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Algorithmic Analog Design and Modeling

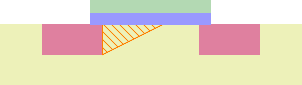
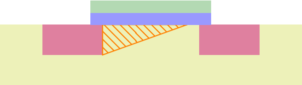
Let's attack the problem of solving power-speed trade-off in conventional analog circuits and come up with an analytical solution:

$$\omega_u = \frac{\mathcal{G}_m \times I_{DS}}{C_L + C_S}$$

Some more information:

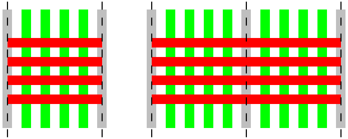
- The main design unknown, I_{DS}.
- ω_u and C_L are given spec parameters,
- $\mathcal{G}_m$ is the main design parameter,
- C_S is a device parameter, related to other device parameters in a complicated way.

Inversion Level of FET Devices

Inversion State		
$\mathcal{G}_m$	High	Low
C_S	Low	High

- **Observation:** Position and shape of channel underneath gate is a function of $\mathcal{G}_m$.

Scaling Effect



W_{eff}	$\times 1$	$\times m$	
I_{DS}	$\times 1$	$\times m$	
$\mathcal{G}_m = g_m / I_D$	$\times 1$	$\times 1$	Invariant
C_S	$\times 1$	$\times m$	
$\mathcal{C}_S = C_S / I_D$	$\times 1$	$\times 1$	Invariant

Remark

In addition to transconductance-efficiency, characteristic capacitance also stays independent of bias current and transistor width.

Analytical Solution

- $\mathcal{C}_s$ is independent of I_{DS} and W, and only a function of $\mathcal{G}_m$.

$$\omega_u = \frac{\mathcal{G}_m I_{DS}}{C_L + I_{DS}\mathcal{C}_S}$$

- Thus, consumption of the circuit can be calculated as below and problem is solved. The only unknown is $\mathcal{G}_m$:

$$I_{DS} = \frac{\omega_u C_L}{\mathcal{G}_m - \omega_u \mathcal{C}_S}$$

Remark

All device parameters are packed into $\mathcal{C}_S$. So, knowing $\mathcal{C}_S$ will reveal everything about circuit's power-speed trade-off.

Summary I

- Speed-power trade-off of a conventional analog circuit can be solved analytically, when a set of proper choices are being made:
  - Design variable: $\mathcal{G}_m$
  - Only device parameter, which is a function of $\mathcal{G}_m$: $\mathcal{C}_S$.
  - The minimum consumption point is:

$$\frac{\partial \mathcal{C}_S}{\partial \mathcal{G}_m} = \frac{1}{\omega_u}$$

Or, equivalently:

$$\frac{\partial \mathcal{G}_m}{\partial \mathcal{C}_S} = \omega_u$$

Summary II

- All device parameters were packed into $\mathcal{C}_S$. So, knowing $\mathcal{C}_S$ will reveal everything about circuit's power-speed trade-off.
- It is very important to note that for estimating bias current of an analog circuit for a target speed requirements, there is no need to know device dimensions and their threshold voltage.

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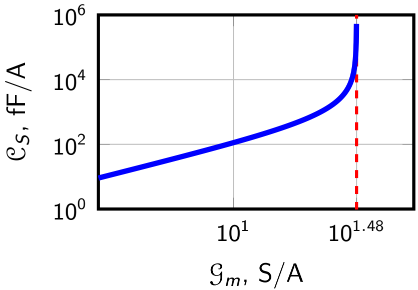
Self-Loading Capacitance

- Self-loading capacitance is the only device parameter which is required to solve the problem.
- Self-loading capacitance can be calculated analytically in strong-inversion region, however a lookup table needs to be created for the entire operating range of a FET device.



Self-Loaded Bandwidth Limitation

Different way of calculating consumption:

$$I_{DS} = I_{DS,0} \times \frac{1}{1 - \frac{\omega_u}{\omega_s}}$$

where,

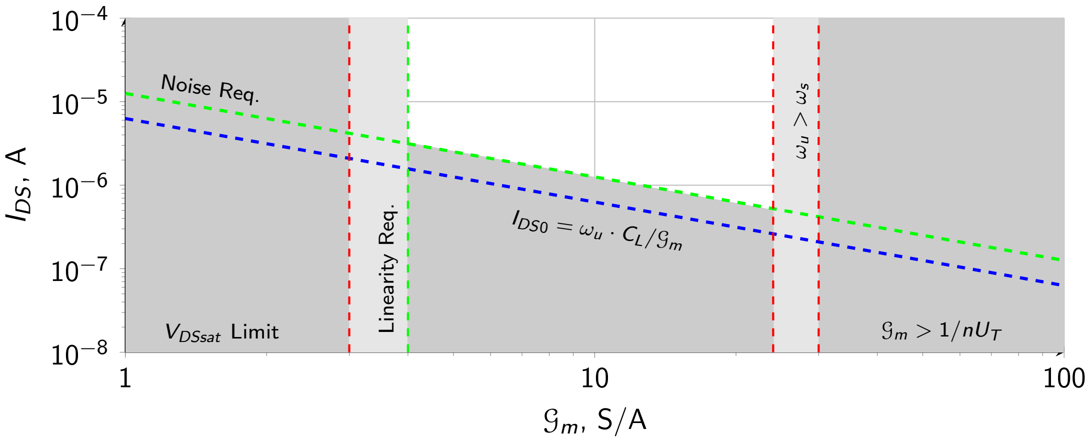
$$I_{DS,0} = \frac{\omega_u C_L}{\mathcal{G}_m}$$

and,

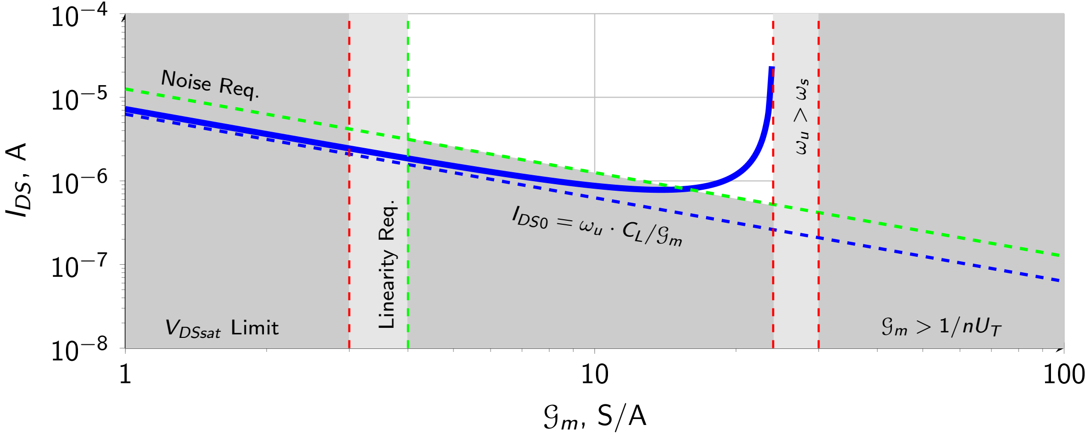
$$\omega_s = \frac{\mathcal{G}_m}{\mathcal{C}_S}$$

which is a technology dependent parameter.

Visual Analysis I

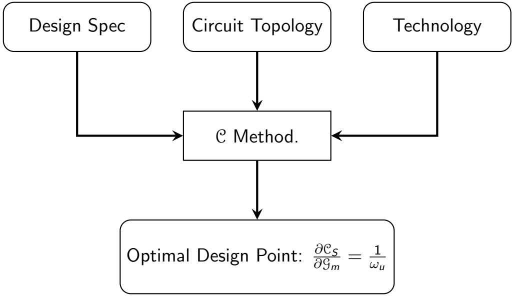


Visual Analysis II

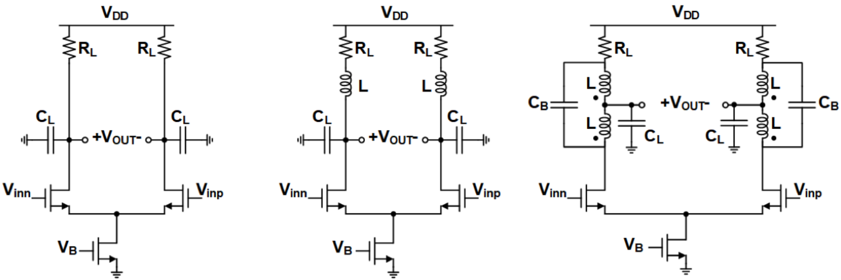


Basic Algorithm

- Design spec can be parameters such as unity gain-bandwidth product, noise, linearity, and supply voltage, among others.
- The key parameter to be extracted from technology is device characteristic capacitance.



Example



Block	Basic Load	RLC Load	T-Coil Load
Consumption	$1\times$	$0.5\times$ to $0.3\times$	$0.25\times$

Also, see: [8].

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Future Work

- Noise and phase noise analysis [13], [15],
- Linearity and supply limitations,
- Design automation [14],
- Theoretical limits of energy consumption for basic analog circuits,
- Analyzing digital logic circuits,
- Analyzing more complex structures, such as ADCs, PLLs, etc.

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Conclusions

- An analytical method was developed to assist designers with a more intuitive approach to develop their analog circuits.
- The underlying relationships will help to devise new circuit design techniques and automation approaches.
- The proposed approach, also enables analyzing architecture level choices.

Conclusions: Further Reading

Topic	References
Theoretical background	[7]
Single-stage amplifiers, inductive peaking	[8]
Ring topologies	[9]
Multi-stage amplifiers	[10]
Inverter based amplifiers	[11]
Discrete-time amplifiers	[12]
Computation complexity	[14]
Noise and phase noise	[13], [15]

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Notes:

- Generally, $\mathrm{g_{moid}}$ is used for $\mathrm{g_m/I_D}$.
- In this report, we use $\mathcal{G}_m$ for $\mathrm{g_m/I_D}$, to be consistent with other ratio parameters, such as $\mathcal{C}_S = C_S/I_D$.

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Acknowledgment

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